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EIA-548
Electronic Design Interchange Format 2.0
Product Code 10 Mar, 1994 COMMITTEE:EDIF
$122.00

EIA-618
Electronic Design Interchange Format (EDIF) Version 3.0
This document defines the syntax and semantics for EDIF Version 3.0, also known as IEC 61690-1. EDIF Version 3.0 is defined at two levels, Level 0 and Level 2. Level 0 is the normal mode of use; Level 2 supports a certain degree of parameterization. EDIF Version 3.0 completely addresses the areas of design connectivity as the ConnectivityView and logical schematics as the schematicView, including at Level 1 the ability to represent schematic and connectivity frames. It represents design hierarchy, library information and design configuration. It also includes capabilities formerly found in the Document and Graphics views of EDIF Version 2.0.
A subsequent release of EDIF, EDIF Version 4.0 (EIA-682-1996), provides support for the domain of printed circuit design and multi-chip modules in addition to the coverage already in EDIF Version 3.0. EDIF 4.0 is upwardly compatible from EDIF Version 3.0. When one purchases EDIF Version 3.0, EDIF Version 4.0 is included.
Product Code 10 Dec, 1993 COMMITTEE:EDIF
$266.00

EIA-682
EDIF Version 4.0 (EIA-682-96) Electronic Design Interchange Format
EDIF Version 4.0 - This document provides the latest version of the standard added support for PCBs and multichip modules, manufacturing drawings and technology rules to the capabilities for schematics connectivity, design hierarchy, libraries, and design configuration already provided by EDIF Version 3.0. EDIF Version 4.0 is fully upwards compatible from EDIF Version 3.0. EDIF Version 4.0 is also known as IEC 61690-2. When one purchases EDIF Version 3.0, EDIF Version 4.0 is included.
Product Code 10 Dec, 1996 COMMITTEE:EDIF
$266.00

EIA/IS-103-A
Library of Parameterized Modules (LPM) Version 2.0
The objective of the LPM standard is to allow efficient access to unique architectures (such as those found in FPGA products) to a wider group of designers who lack a detailed knowledge of the vendor’s silicon architecture. This access is provided via synthesis tools and other design entry systems.

Through the LPM standard, designs can remain technology-independent longer. The user is freed from the need to know or decide upon the implementation technology until later in the design flow. The designer’s entry tools can be completely independent of the target technology and rely on synthesis tools to map the design to the target technology. The objective of LPM is to provide a generic, technology independent set of logical primitives with which to construct a design and get efficient performance from a wide array of technologies.
Product Code 10 Feb, 1999 COMMITTEE:EDIF
$201.00

I/O BUFFER INFORMATION SPECIFICATION (IBIS)
EIA-656-A
IBIS is a consistent, software-parsable format to be used by semiconductor vendors for specifying the analog characteristics of input and output buffers of digital semiconductor devices. This essential information is readily transformed into accurate models by EDA vendors and semiconductor customers. Resulting behavioral models enable users to perform high-speed, accurate signal-integrity simulations of their digital system interconnects. Prior to IBIS, I/O buffer model development methodologies revealed proprietary device fabrication process information.
Product Code 10 Sep, 1999 COMMITTEE:IBIS
$106.00

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VHDL

EIA-567-A
VHDL Hardware Component Modeling and Interface Standard (ANSI/EIA-567-A-95)
The purpose of this standard is to provide guidelines for the production of VHDL models for hardware descriptions that:

a) conform to a common signal interface convention;

b) possess common simulation capabilities;

c) are reusable as library elements of other designs;

d) support multiple source procurement; and

e) support technology independent reprocurement.

It is not the purpose of this standard to create models that promote a particular hardware design methodology.

Product Code 10 Jul, 1995 COMMITTEE:VHDL
$61.00